WHAT IS CLAIMED IS:

1. A processor comprising:

a data memory for storing data;

a set of instructions that are executed by said processor, said instructions including addressing modes to reference data stored in said data memory;

a programmable address arithmetic unit (programmable AAU) providing logic functions, said logic functions specified by data stored in an programmable AAU memory;

one or more configuration instructions to load configuration data into said programmable AAU memory;

one or more registers, each register configured to hold an address into said data memory, said registers operatively coupled to said programmable AAU such that said programmable AAU can modify said address into said data memory held in each of said registers; and

an instruction decoder responsive to said instructions and said addressing modes, wherein output bits of said instruction decoder are coupled as inputs to said programmable AAU to control the modification of an address stored in said one or more registers.

2. The processor of Claim 1, wherein said AAU memory is loaded with data as part of an initial boot-up of said processor from a boot memory.

3. The processor of Claim 1, wherein said AAU memory is loaded by using a direct memory access channel from said data memory.

4. The processor of Claim 1, wherein said programmable AAU comprises a micro-sequencer capable of performing multi-cycle operations.

5. The processor of Claim 1, wherein said programmable AAU comprises a programmable logic array.

6. The processor of Claim 1, wherein said programmable AAU comprises a field programmable gate array.

7. The processor of Claim 1, wherein said programmable AAU comprises a cross-bar switch configured to receive an input word comprising a plurality of bits and to produce an output word by programmably re-arranging the bits in said input word.

8. A processor, comprising:

a program memory storing first instructions;

a data memory storing data;

an arithmetic unit connected to said program memory and said data memory and performing arithmetic manipulations on said data in accordance with said first instructions;

an address program memory storing second instructions;

an address memory storing addresses which access said data in said data memory; and

an address arithmetic unit connected to said address program memory and said address memory and performing arithmetic manipulations on said addresses in accordance with said second instructions to generate new addresses which access said data in said data memory.

9. The processor of Claim 8, wherein said address memory comprises one or more registers.

10. The processor of Claim 8, wherein said address memory comprises one or more address registers.

11. The processor of Claim 8, wherein said address arithmetic unit is responsive to said first instructions.

12. The processor of Claim 8, wherein data is stored in said address arithmetic unit memory by using said first instructions.

13. The processor of Claim 8, wherein data loaded into said address arithmetic unit memory modifies one or more of said first instructions.

14. The processor of Claim 8, wherein said address arithmetic unit memory is loaded by using a direct memory access channel from said data memory.

15. The processor of Claim 8, wherein said address arithmetic unit comprises a micro-sequencer capable of performing multi-cycle operations.

16. The processor of Claim 8, wherein said address arithmetic unit comprises a programmable logic array.

17. The processor of Claim 8, wherein said address arithmetic unit comprises a field programmable gate array.

18. A method of operating a processor which includes a main ALU and memory, comprising:

providing a programmable address computational unit separate from said ALU; and

providing addresses into said memory for said ALU from said programmable address computation unit.

19. The method of Claim 18, wherein said programmable address computational unit is responsive to auto-update addressing modes of a first instruction set of said processor.

20. The method of Claim 18, wherein said step of providing a programmable address computational unit comprises the step of loading data into a programmable address computational unit memory.

21. The method of Claim 20, wherein said processor provides instructions to perform said step of loading data into an address computational unit memory.

22. The method of Claim 18, wherein said addresses are stored in registers.

23. The method of Claim 18, wherein said programmable address computation unit is a programmable logic device which is programmed by loading data into an address computational unit memory.

24. A method for programming a user programmable address arithmetic unit, comprising the steps of:

writing a first program in a first programming language, said first program configured to implement one or more address calculation functions in an address arithmetic unit ; and

compiling said first program;

generating a first executable image, said first executable image adapted for loading into a address arithmetic unit program memory of an address arithmetic unit in a processor having a programmable address arithmetic unit.

writing a second program in a second programming language, said second program configured to implement a desired digital signal processing algorithm;

compiling said second program into object code for said processor, said object code comprising a plurality of machine level instructions for said processor, said plurality of machine level instructions comprising instructions to control said programmable address arithmetic unit; and

generating a second executable image, said second executable image adapted for loading into a program memory of said processor.

25. The method of Claim 24, wherein said address calculation function is invoked by an auto-update addressing mode.

26. The method of Claim 24, wherein said first programming language is a hardware definition language.

27. The method of Claim 26, wherein said second programming language is an assembly language.

28. The method of Claim 26, wherein said second programming language is a high level programming language.

29. The method of Claim 24, wherein said address arithmetic unit provides special purpose circuitry, said method further comprising the step of adapting said first program to use a software library to access said special purpose circuitry.

30. An apparatus comprising:

very long instruction word processor having multiple functional units that receive different dispatched portions of a very long instruction word wherein one or more of said functional units comprise a user programmable address arithmetic unit; and

a load-store unit comprising an instruction decoder responsive to a field of said very long instruction word, said field being sent to and instruction decoder by a dispatch unit.

31. A processor comprising:

a data memory, said data memory storing data;

a set of instructions that are executed by said processor, said instructions including addressing modes to reference data stored in said data memory;

an address arithmetic unit means for providing address calculations using instructions stored in an address arithmetic unit memory, said address arithmetic unit means capable of calculating one or more new addresses per clock cycle.

32. The processor of Claim 31, further comprising configuration means for loading data into said address arithmetic unit memory.